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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,344	03/31/2000	Carl M. Ellison	042390.P8098	1432

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EXAMINER	
GURSHMAN, GRIGORY	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/539,344	ELLISON C.	
	Examiner	Art Unit	
	Grigory Gurshman	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/29/04 and 7/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The formal drawings filed on 6/11/04 are accepted by Examiner.

Response to Arguments

2. Claims 1-14, 16-19, 21-22, 24-34, 36-39, 61-74, and 76-79 have been amended. Claims 81-99 have been added. All of the instant claims are addressed in the rejection section of the instant Office Action.

3. Referring to claims 1-80, Applicant argues that neither Greenstein nor Branigan discloses or suggests a processor executive that, when executed no the processor, loads and operating system executive on the platform. Applicant argues that the CPU of Greenstein clearly is not the "processor executive" claimed by Applicant. Examiner respectfully disagrees and points out, that one of ordinary skill in the art, using broad but reasonable interpretation of the claim, would have equated the CPU, which controls the operating system, with the "processor executive" claimed by Applicant. Applicant claims do not reflect any patentably distinguishable differences between the claimed invention and Greenstein with respect to the "processor executive".

4. With regard to independent claims 1, 21, 61 and 81, Applicant further argues that even if Greenstein and Branigin were to be combined, the combination would not render the instant claims obvious. Examiner respectfully disagrees and points out that the combination of Greenstein and Branigin does render the instant claims obvious for the following reasons:

While Greenstein does not explicitly teach the use of PE identifier to identify the PE to the operating system it is trying to access, Branigin teaches that CPU ID is used for accessing a Storage Unit through the M-BUS (see column 18, lines 43-63). Therefore, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Greenstein, which uses the processor for accessing the isolated memory area with the key, by adding the processor identifier as taught in Branigin. One of ordinary skill in the art would have been motivated to use the processor for accessing the isolated memory area with the key and the processor identifier as taught in Branigin in order for Main Storage Units (MSU) top accept data from M-BUS (see Branigin, column 18 line 60-64).

5. Applicant also argues that neither Greenstein nor Branigin teach a processor that can operate in normal and isolated execution mode. Examner points out that the limitation "processor operating in an isolated execution mode" is met by the CPU (101), which is connected to the security devices (105 and 110). The "normal execution mode" is met by the CPUSKs 309 (in Fig.3), which do not protect against storage alteration by I/O channel programs (see Greenstein).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenstein (U.S. Patent No. 5.809.546) in view of Branigin (U.S. Patent No. 4.419.724).

8. Referring to the instant claims, Greenstein discloses a method for managing I/O (input /output) buffers in shared storage, including storage keys for controlling accesses to the buffers (see abstract and Fig. 1). Greenstein teaches protecting the storage within the computer system against unwanted CP (central processor) access. Greenstein also teaches the use of CP keys provided for protecting against unwanted accesses by any CP in the system. The I/O keys must be supported by a hardware I/O storage array when only real (or absolute) addressing is used by I/O programs. However, the CP keys may be supported by either real CP keys in a second hardware key array; or alternatively the CP keys may be provided as virtual CP keys in a field in each page table entry (which is used for translating CP virtual addresses to CP real addresses) – see abstract and Figs. 1-6).

9. Referring to the independent claims 1, 21, 41, 61, 81 and claims 16, 36, 56, 18, 38, 58, 76 and 78, the limitation "a processor executive to handle an operating system executive (OSE) in a secure environment" is met by CPU (101 in Fog.1) which handles the main storage (106) within the operation system of the computer system 100. The secure environment is provided buy a storage controller (105 in Fig.1) connected with the storage protection array (110). The limitation " the secure environment having a fused key (FK) and associated with an isolated memory area in a platform" is met by a storage protection array (110) with keys (see Fig 4A, units 402-406). The storage array is associated with an isolated memory area (114 in Fig.1). Greenstein teaches the

computer system (100 in Fig. 1), which has operation system and subsystems (104). Referring to the limitation "processor operating in an isolated execution mode" is met by the CPU (101), which is connected to the security devices (105 and 110). The "normal execution mode" is met by the CPUSKs 309 (in Fig.3), which do not protect against storage alteration by I/O channel programs.

The limitation "a PE handler to handle the PE using FK and the PE supplement" is met by CPU (101) and storage controller (105) and the CPU key (309) – see Fig.3.

10. Greenstein, however, does not explicitly teach the use of PE identifier to identify the PE to the operating system it is trying to access. Referring to the instant claims, Branigin discloses a main bus interface package (see abstract). Branigin teaches that Central Processors (CPU) is connected to an M BUS with the Main Storage Processors (MSP). As a typical operation, the CPU might wish to communicate with an MSU. The CPU would contend for priority on the M-BUS and when granted access might place on the M-BUS a word wherein byte 1 contains the destination ID. The function code in byte 0 of the word placed on the M-BUS might tell the MSP that it should retrieve data from main storage. Branigin teaches that CPU ID is used for accessing a Storage Unit through the M-BUS (see column 18, lines 43-63). Therefore, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Greenstein, which uses the processor for accessing the isolated memory area with the key, by adding the processor identifier as taught in Branigin. One of ordinary skill in the art would have been motivated to use the processor for accessing the isolated memory area with the key and the processor identifier as taught in Branigin.

in order for Main Storage Units (MSU) top accept data from M-BUS (see Branigin, column 18 line 60-64).

11. Referring to claims 2, 22, 42 and 62, it is well known in the art to have a processor to access the boot-up code of the platform from the isolated area of the platform memory. For example it is done in most of the computers, wherein boot-up code is invoked by the processor from the isolated ROM area of BIOS. One of ordinary skill in the art would have been motivated to use the boot-up code stored in the isolated memory area in a platform for proper operation of OS of the platform.

12. Referring to claims 3, 23, 43 and 63, Branigin teaches granting IDs to CPU as well as to storage areas of OS (see Fig.8), which meets the limitations recited in the instant claims.

13. Referring to claims 4, 7, 24, 27, 44, 47, 64, 67 and 17, 37, 57, 77 and 83, Branigin teaches verifying the identifier of the CPU (see column 18, lines 43-63). Greenstein also shows verification of the key identifying the I/O or a processor (see Fig.21), which meets the limitations recited in the instant claims.

14. Referring to claims 5, 8, 25, 28, 45, 48, 65, 68 and 87, the limitation "PE key generator" is met by Figs. 7 and 8 of Greenstein. CPU keys are used for logging into the mains storage (106 in Fig. 1).

15. Referring to claims 6, 26, 46 and 66, the limitation "a PE key combiner" is met by CPU ID combined with the signal in the ANDs and ORs units (see Branigin, column 16, lines 40-50).

16. Referring to claims 10, 30, 50 and 70, the limitation "a module loader" is met by I/O buffers (114 in Fig.1 of Greenstein). The "interface handler" is met by the storage controller (105). The "page manager" is met by the page table (107 in Fig.2).

17. Referring to claims 13, 33, 53 and 73, the limitations recited in the instant claims are taught in Branigin (column 16, lines 40-50). Branigin teaches CPU ID or OS unit ID combined with the signal in the ANDs and ORs units.

18. Referring to claims 14, 34, 54 and 74, Greenstein teaches the use of "the isolated create instruction " in a form of protection (SIOP) instruction (see Fig. 7).

19. Referring to claims 15, 35, 55, 75 and 97, Greenstein teaches the use of a storage protection array (110 in Fig. 8), which meets the "atomic sequence" recited in the instant claims.

20. Referring to claims 19, 20, 39, 40, 59, 60, 79, 80 and 99, it is well known in the art to have a chipset including memory controller hub and an input output controller hub.

For example HP computers have chipsets with the memory controller hub and an input output controller hub.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grigory Gurshman whose telephone number is (703) 306-2900. The examiner can normally be reached on 9 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (703) 305-1830. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Examiner
Art Unit 2132

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